REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 1-9, and 11-46 are pending in the present application.

The drawings are objected to.

The specification is objected to because of informalities.

Claim 38 is rejected under 35 U.S.C. §112, second paragraph.

Claims 1-46 are rejected under 35 U.S.C. §101.

Claims 1-4, 6-23, 26-32 are rejected under 35 U.S.C. §102(a) as being unpatentable over U.S. Patent No. 6,121,223 ("Okamoto").

Claims 21, 26, and 27-32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Okamoto in view of U.S. Patent No. 5,715,276 ("Tran").

Claims 5, 24, 25, and 45 are objected to.

Claims 16, 24, 28, and 36 have been canceled.

Claims 1, 6, 14, 17, 26, 33-34, 38-40, and 46 have been amended.

Claims 47-50 have been added.

Support for amended claims 1, 6, 14, 17, 26, 33-34, 38-40, and 46, and new claims 47-50 is found on page 1, lines 16-18, and page 11, lines 24 through page 12, line 2, page 17, lines 16-19, s 4-28 of the specification, page 21, line 8 through page 27, line 21, Figures 1-3, and 7a-9b, and claims 1-46 as originally filed. No new matter has been added.

The Office Action mailed 12/15/2006 states that "the drawing(s) filed on 27 December 2005 is/are ... objected to" (12/15/2006 Office Action, p. 1). The Office Action mailed 12/15/2006 further states that

> It is office policy to request from applicants that submitted figures contain both text and numerical labels to allow individuals viewing each figure to be able to determine the designation of each element in the figure without having to go into the specification.

(12/15/2006 Office Action, p. 2).

Applicant submits that no drawings were filed on December 27, 2005. The only drawings that were filed for the current application were the original drawings filed on June 26, 2001. These original drawings were accepted by the patent office as reflected in the Office Action mailed 9/23/2005 on page 1.

Applicant has reviewed the requirements for drawings as outlined in 37 C.F.R. 1.84 and in MPEP 608.02(e) and submits that the drawings for the present application are in compliance with current regulations.

Nevertheless, Figures 2, 3, 7a-7b, 8a-8b, and 9a-9b have been amended. Replacement sheets for Figures 2, 3, 7a-7b, 8a-8b, and 9a-9b are submitted following the last page of this response. Applicant submits that the Figures comply with 37 C.F.R. 1.84 and MPEP 608.02(e). Applicant respectfully requests that if the Office believes that any particular drawing in the present application is not in compliance with the current regulation, that the Office cite the specific regulation.

The specification is objected to because of informalities.

The specification has been amended at pages 2, 3, 10, and 13 to include the suggestions made by the Office. No new matter has been added.

Applicant submits that in view of the amendment to the specification, the objection to the specification has been overcome.

Claim 38 is rejected under 35 U.S.C. §112, second paragraph.

As stated above, claim 28 has been amended. Support for amended claim 28 is found in claims 11, 19, 31, and 33 as originally filed.

Applicant submits that in view of the amendment to claim 38, the rejection under 35 U.S.C. §112, second paragraph has been overcome.

Claim 1-46 has been rejected under 35 U.S.C. §101. The Office Action mailed 12/15/2006, however, merely cites exerts from MPEP 2106 IV C 2 (2), pages 2100-11 and 2100-12, without applying them to the claims and without presenting a prima facie case of unpatentability.

Applicant submits that "The examiner bears the initial burden... of presenting a prima facie case of unpatentability... After USPTO personnel identify and explain in the record the reasons why a claim is for an abstract idea with no practical application, then the burden shifts to the applicant to either amend the claim or make a showing of why the claim is eligible for patent protection." MPEP 2106 IV D, page 2100-13. Applicant respectfully submits that the Office has failed to present a prima facie case of unpatentability under 35 U.S.C. §101.

Nevertheless, claims 1, 6, 14, 26, 33, 39, and 46 have been amended to facilitate prosecution of this case. Applicant submits that claims 1-9, and 11-50 produce a useful, concrete, and tangible result. If the Office believes otherwise, Applicant requests that the Office clearly communicate its findings, conclusions, and bases as it is required to under MPEP 2106 VII, page 2100-15.

Claims 1-9, and 10-46 are rejected under 35 U.S.C. §102(a) and §103(a) as being unpatentable over Okamoto and Tran.

It is submitted that Okamoto and Tran do not render claims 1-9, and 10-49 unpatentable under 35 U.S.C. §102(a) or §103(a).

Okamoto includes a disclosure of a spread spectrum communications system with a method and apparatus provided for reducing transmission error and power consumption despite an increase in sampling. There are serially provided 4k (k denotes a spreading factor) shift registers (1) to (4) to deal with at most four samples to develop input spread signals, which are multiplied by spread-code replica signals from a replica generator. Sums .pi.1 to .pi.4 of respective k products are obtained. An output of a correlator is obtained by further adding the sums. At this time, the shift registers (1) to (4), adders and the replica generator are controlled in

response to a control signal depending upon the number of samples. When three samples are sampled for one chip, the shift register (4) is disabled and (1, 1, 1, -1, -1, -1, 1, 1, 1, 1, 1, 1, -1, -1, -1, NA, NA, NA, NA, NA) are prepared as a replica and only adder .pi.4 is disabled and an output of the correlator is obtained from signals stored in the shift registers (1), (2), (3) (See Okamoto Abstract).

Tran includes a disclosure of a scaleable architecture for implementing a large bit matched filter. The implementation of the bit matched filter requires less silicon and consumes less power as compared to the existing design. An effective way to turn the bit matched filter on and off for power saving is also disclosed (See Tran Abstract).

It is submitted that Okamoto and Tran do not teach or suggest determining first intermediate correlation values for a first plurality of sample sequences during a first clock cycle, determining second intermediate correlation values for the first plurality of sample sequences during a second clock cycle, determining correlation outputs for the first plurality of sample sequences from the first and second intermediate correlation values, and determining a synchronization point that identifies an amount of delay incurred from transmission of the sample sequences from the correlation outputs.

On the contrary, Figure 7 of Okamoto discloses generating a correlator output at 51. The correlator output is the added products from adders 41-1, 41-2, 41-3, and 41-4. The products from adder 41-1 is the sum of a first set of samples from shift register (1)11-1 multiplied by replica signals by multipliers 31-1a to 31-1k. The products from adder 41-2 is the sum of a second set of samples from shift register (2)11-2 multiplied by replica signals by multipliers 31-2a to 31-2k. The products from adder 41-3 is the sum of a second set of samples from shift register (3)11-3 multiplied by replica signals by multipliers 31-3a to 31-3k. The products from adder 41-4 is the sum of a second set of samples from shift register (4)11-4 multiplied by replica signals by multipliers 31-4a to 31-4k. Thus, the products from adders 41-1, 41-2, 41-3, and 41-4 are each generated from unique samples (see Okamoto col. 9, lines 14-26 and Figure 7). The

products are not intermediate correlation values determined for the same plurality of sample sequences but each product is determined from unique sets of samples for different shift registers.

Similarly, Figure 8 of Okamoto discloses generating a correlator output at 52. The correlator output is added products from adders 42-1, 42-2, 42-3, and 42-4. The products from each of the adders are also each generated from unique samples (see Okamoto col. 10, lines 9-18 and Figure 8). The products are not intermediate correlation values determined for the same plurality of sample sequences.

Furthermore, the products from adders 41-1, 41-2, 41-3, and 41-4 shown in Figure 7 and from adders 42-1, 42-2, 42-3, and 42-4 shown in Figure 8 are not illustrated or described to be generated at different clock cycles. Thus, the products from the adders are not a first intermediate correlation value determined for a first plurality of sample sequences during a first clock cycle and a second intermediate correlation value determined for a second plurality of sample sequences during a second clock cycle.

In addition, the Office Action mailed 12/15/2007 states that

> Okamoto further discloses determining a correlation output for each of the sample sequences; and determining a synchronization point for the code sequence from the correlation outputs (col. 12, lines 36-63).

(12/15/2006 Office Action, p. 9).

Applicant submits that the cited text from the Office states in part that

> A window control unit 11 is controlled by the synchronization pulses and by correlation signals (of several samples in front of and in rear of the window) which are gated by the control unit 11.

(Okamoto col. 12, lines 46-49)

Applicant submits that having a window control unit "controlled by the synchronization pulses and by correlation signals" is not the same as determining a synchronization point that

identifies an amount of delay incurred from transmission of sample sequences from correlation outputs, as required by the claimed invention.

Tran only discloses a symbol-matched filter having a low silicon and power requirement. Tran does not teach or suggest determining first intermediate correlation values for a first plurality of sample sequences during a first clock cycle, determining second intermediate correlation values for the first plurality of sample sequences during a second clock cycle, determining correlation outputs for the first plurality of sample sequences from the first and second intermediate correlation values, and determining a synchronization point that identifies an amount of delay incurred from transmission of the sample sequences from the correlation outputs.

In contrast, claim 1 states

> A method for managing a code sequence, comprising:
> determining first intermediate correlation values for a first plurality of sample sequences during a first clock cycle;
> determining second intermediate correlation values for the first plurality of sample sequences during a second clock cycle;
> determining correlation outputs for the first plurality of sample sequences from the first and second intermediate correlation values; and
> determining a synchronization point that identifies an amount of delay incurred from transmission of the sample sequences from the correlation outputs

(Claim 1 as amended) (Emphasis added).

Given that claims 2-5 and 47 depend from claim 1, it is likewise submitted that claims 2-5 and 47 are also patentable under 35 U.S.C. §102(a) and §103(a) over Okamoto and Tran.

It is further submitted that Okamoto and Tran do not teach or suggest processing a first group of coefficients in the code sequence, loaded in a plurality of code sequence registers during a first clock cycle, with a first group of contiguous sample values in a received sample to determine a first intermediate correlation value during the first clock cycle, processing a second group of coefficients in the code sequence, loaded in the

plurality of code sequence registers previously used for the first group of coefficients during a second clock cycle, with a second group of contiguous sample values in the received sample to determine a second intermediate correlation value during the second clock cycle, determining a correlation output from the first and second intermediate correlation values, and determining a synchronization point that identifies an amount of delay incurred from transmission of the sample values from the correlation output.

On the contrary, Okamoto discloses determining intermediate correlation values by processing replica signals generated by and stored in replica generator 21. As shown in Figure 7, a first group of replica signals are transmitted from first locations in the replica generator 21 along dedicated lines to specific multipliers 31-1a to 31-1k. These products are summed by adder 41-1 to generate a first product. A second group of replica signals are transmitted from second locations in the replica generator 21 along dedicated lines to specific multipliers 31-2a to 31-2k. These products are summed by adder 41-2 to generate a second product. A third group of replica signals are transmitted from third locations in the replica generator 21 along dedicated lines to specific multipliers 31-3a to 31-3k. These products are summed by adder 41-3 to generate a third product. A fourth group of replica signals are transmitted from fourth locations in the replica generator 21 along dedicated lines to specific multipliers 31-4a to 31-4k. These products are summed by adder 41-4 to generate a third product. Neither the second, third, nor fourth groups of replica signals in Okamoto are loaded into a plurality of code sequence registers previously used for the first group of replica signals. These groups of replica signals are transmitted on dedicated lines from their unique locations in the replica generator to multipliers 31-2a to 31-2k, 31-3a to 31-3k, and 31-4a to 31-4k (see Okamoto, col. 9, lines 18-26, and Figure 7).

Figure 8 illustrates processing samples from shift registers 12-1 to 12-4 with a same group of replica signals from replica generator 22 to generate results to be summed

by adders 42-1 to 42-4. Applicant submits that Figure 8 of Okamoto does not teach or suggest processing a first group of coefficients in the code sequence with a first group of contiguous sample values in a received sample to determine a first intermediate correlation value and processing a second group of coefficients in the code sequence with a second group of contiguous sample values in the received sample to determine a second intermediate correlation value. Figure 8 of Okamoto illustrates processing the same group of replica signals form the replica generator 22 with samples from each of the shift registers 12-1 to 12-4 (see Okamoto col. 10, lines 12-14 and Figure 8).

Furthermore, the products from adders 41-1, 41-2, 41-3, and 41-4 shown in Figure 7 and from adders 42-1, 42-2, 42-3, and 42-4 shown in Figure 8 are not illustrated or described to be generated at different clock cycles. Thus, the products from the adders are not a first intermediate correlation value determined from a first group of coefficients in the code sequence during a first clock cycle and a second intermediate correlation value determined for a second group of coefficients in the code sequence during a second clock cycle.

In addition, the Office Action mailed 12/15/2007 states that

> Okamoto further discloses determining a correlation output for each of the sample sequences; and determining a synchronization point for the code sequence from the correlation outputs (col. 12, lines 36-63).

(12/15/2006 Office Action, p. 9).

Applicant submits that the cited text from the Office states in part that

> A window control unit 11 is controlled by the synchronization pulses and by correlation signals (of several samples in front of and in rear of the window) which are gated by the control unit 11.

(Okamoto col. 12, lines 46-49)

Applicant submits that having a window control unit "controlled by the synchronization pulses and by correlation signals" is not the same as determining a synchronization point that

identifies an amount of delay incurred from transmission of sample sequences from correlation outputs, as required by the claimed invention.

Tran only discloses a symbol-matched filter having a low silicon and power requirement. Tran does not teach or suggest processing a first group of coefficients in the code sequence, loaded in a plurality of code sequence registers during a first clock cycle, with a first group of contiguous sample values in a received sample to determine a first intermediate correlation value during the first clock cycle, processing a second group of coefficients in the code sequence, loaded in the plurality of code sequence registers previously used for the first group of coefficients, with a second group of contiguous sample values in the received sample to determine a second intermediate correlation value during the second clock cycle, determining a correlation output from the first and second intermediate correlation values, and determining a synchronization point that identifies an amount of delay incurred from transmission of the sample values from the correlation output.

In contrast, claim 6, as amended, states

> A method for managing a code sequence, comprising:
> processing a first group of coefficients in the code sequence, loaded in a plurality of code sequence registers during a first clock cycle, with a first group of contiguous sample values in a received sample to determine a first intermediate correlation value during the first clock cycle;
> processing a second group of coefficients in the code sequence, loaded in the plurality of code sequence registers previously used for the first group of coefficients during a second clock cycle, with a second group of contiguous sample values in the received sample to determine a second intermediate correlation value during the second clock cycle;
> determining a correlation output from the first and second intermediate correlation values; and
> determining a synchronization point that identifies an amount of delay incurred from transmission of the sample values from the correlation output.

(Claim 6 as amended) (Emphasis added).

Given that claims 7-9, 11-13, and 48-49 depend directly or indirectly from claim 6, it is likewise submitted that claims 7-9, 11-13, and 48-49 are also patentable under 35 U.S.C. §102(a) and §103(a) over Okamoto and Tran.

Applicant further submits that Okamoto and Tran do not teach or suggest organizing a code sequence, having L contiguous coefficients, into L/n contiguous code sequence groups having n coefficients each, selecting a number of sample sequences to process in parallel where each of the sample sequences has contiguous sample values from a received sample, organizing contiguous sample values from each of a first set of contiguous sample sequences to process in parallel into a first set of contiguous sample sequence groups, processing coefficients in each of the code sequence groups in parallel with corresponding sample values in corresponding sample sequence groups from the first set of sample sequences, where each of code sequence groups is processed during a different clock cycle, determining a correlation output for each of the sample sequences, and determining a synchronization point that identifies an amount of delay incurred from transmission of the sample sequences from the correlation output.

On the contrary, Applicant submits that the limitation of organizing the code sequence by "organizing the code sequence into L/n groups" was previously recited in claim 24 which was objected to in the Office Action mailed 12/15/2006. The Office Action mailed 12/15/2006 does not provide any grounds of rejection for claim 24.

In addition, the Office Action mailed 12/15/2007 states that

> Okamoto further discloses determining a correlation output for each of the sample sequences; and determining a synchronization point for the code sequence from the correlation outputs (col. 12, lines 36-63).

(12/15/2006 Office Action, p. 9).

Applicant submits that the cited text from the Office states in part that

> A window control unit 11 is controlled by the synchronization pulses and by correlation signals (of several samples in front of and in rear of the window) which are gated by the control unit 11.

(Okamoto col. 12, lines 46-49)

Applicant submits that having a window control unit "controlled by the synchronization pulses and by correlation signals" is not the same as determining a synchronization point that identifies an amount of delay incurred from transmission of sample sequences from correlation outputs, as required by the claimed invention.

Tran only discloses a symbol-matched filter having a low silicon and power requirement. Tran does not teach or suggest organizing a code sequence, having L contiguous coefficients, into L/n contiguous code sequence groups having n coefficients each, selecting a number of sample sequences to process in parallel where each of the sample sequences has contiguous sample values from a received sample, organizing contiguous sample values from each of a first set of contiguous sample sequences to process in parallel into a first set of contiguous sample sequence groups, processing coefficients in each of the code sequence groups in parallel with corresponding sample values in corresponding sample sequence groups from the first set of sample sequences, where each of code sequence groups is processed during a different clock cycle, determining a correlation output for each of the sample sequences, and determining a synchronization point that identifies an amount of delay incurred from transmission of the sample sequences from the correlation output.

In contrast, claim 14, as amended, states

> A method for managing a code sequence, comprising:
> organizing the code sequence, having L contiguous coefficients, into L/n contiguous code sequence groups having n coefficients each;
> selecting a number of sample sequences to process in parallel where each of the sample sequences has contiguous sample values from a received sample;
> organizing contiguous sample values from each of a first set of contiguous sample sequences to process in parallel into a first set of contiguous sample sequence groups;
> processing coefficients in each of the code sequence groups in parallel with corresponding sample values in corresponding sample sequence groups from the first set of sample sequences, where each of code sequence groups is processed during a different clock cycle;

> determining a correlation output for each of the sample sequences; and
> determining a synchronization point that identifies an amount of delay incurred from transmission of the sample sequences from the correlation output.

(Claim 14, as amended) (Emphasis added).

Claims 26, 33, 39, and 46 include similar limitations.

Given that claims 15-25, and 50 depend directly or indirectly from claim 14, claims 27-32 depend directly or indirectly from claim 26, claims 34-38 depend directly or indirectly from claim 33, and claims 40-45 depend directly and indirectly from claim 39, it is likewise submitted that claims 15-25, 27-32, 34-38, 40-45, and 50 are also patentable under 35 U.S.C. §102(a) and §103(a) over Okamoto and Tran.

Applicant further submits that Okamoto and Tran do not teach or suggest determining a synchronization point comprises identifying a correlation output having a highest numerical value.

The Office Action mailed 12/15/2006 states in part that

> Okamoto further discloses wherein determining a synchronization output comprises determining a correlation output having a highest numerical value (col. 12, lines 36-63).
> Examiner asserts wherein a highest numerical value corresponds to some threshold value.

(12/15/2006 Office Action, p. 9).

As earlier discussed, Applicant submits having a window control unit "controlled by the synchronization pulses and by correlation signals" is not the same as determining a synchronization point that identifies an amount of delay incurred from transmission of sample sequences from correlation outputs, as required by the claimed invention.

Furthermore, the text cited by the Office states in part that

> The correlation signals in the window (time window) are compared with thresholds which are preset for respective samples by comparators 12-1 to 12-5.

(Okamoto col. 12, lines 56-58).

Applicant submits that comparing correlation signals with thresholds is not the same as identifying a correlation output having a highest numerical value. For example, comparing correlation signals with thresholds may yield more than one differing result when more than one differing correlation signal exceeds the threshold. Furthermore, comparing correlation signals with thresholds do not necessarily yield a correlation output having the highest numerical value.

Tran only discloses a symbol-matched filter having a low silicon and power requirement. Tran does not teach or suggest determining a synchronization point comprises identifying a correlation output having a highest numerical value.

In contrast, claim 47 states

> The method of Claim 1, wherein determining the synchronization point comprises identifying a correlation output having a highest numerical value.

(Claim 47) (Emphasis added).

Claims 17, 29, 37, 43, 49 include similar limitations.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-9, and 11-50 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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Lawrence M. Cho
Attorney for Applicant
Registration No. 39,942

P.O. Box 2144
Champaign, IL 61825
(217) 377-2500